

⁸
REPLACED BY
ART 34 AMDT

10/523517

Claims

1. A data processing system having:

at least one processor chip including a processor unit and an internal data cache, and
- 5 a dummy interface which receives data written to it by the processor chip, and discards it.
2. A data processing system according to claim 1 in which the dummy interface is coupled to a memory, the dummy interface passing data to the processor chip during initialisation.
- 10 3. A data processing system according to claim 1 further including one or more further processing chips which have read/write access to external memory.
4. A method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting write instructions
15 out of the integrated circuit for updating an external memory, the method including discarding the write instructions and arranging for the program code operated by the processor to require only the data cache as memory.